In the Claims:

1. (Original) A method of forming isolating regions of a semiconductor device, the method comprising:

providing a workpiece, the workpiece having at least one first region and at least one second region, the at least one first region comprising at least one first active area, the second region comprising areas for at least one second active area, the workpiece having a top surface;

patterning the first region with at least one first trench, the first trench having sidewalls, a bottom, and a first depth within the workpiece;

forming a first insulating layer over the at least one first trench sidewalls and bottom;

depositing a semiconductive material in the at least one first trench over the first insulating layer, wherein the semiconductive material is recessed beneath the workpiece top surface;

patterning the second region with at least one second trench, the second trench having a second depth within the workpiece, wherein the second depth is less than the first depth;

depositing an insulating material in the at least one second trench and in the semiconductive material recess of the at least one first trench; and

forming at least one second active area in the second region.

2. (Original) The method according to Claim 1, wherein the at least one first active area comprises at least one high voltage device, and wherein the at least one second active area comprises at least one low voltage device.

3. (Original) The method according to Claim 1, wherein patterning the first region with at least one first trench comprises forming deep trenches, wherein patterning the second region with at least one second trench comprises forming shallow trench isolation regions, and wherein depositing an insulating material in the semiconductive material recess of the at least one first trench comprises forming shallow trench isolation over the deep trenches.

4. (Original) The method according to Claim 1, wherein depositing a semiconductive material comprises depositing doped polysilicon or undoped polysilicon, wherein forming the insulating layer over the at least one first trench sidewalls and bottom comprises:

forming a thin nitride layer over the at least one first trench sidewalls and bottom; and

forming a thin oxide layer over the thin nitride layer.

5. (Original) The method according to Claim 1, further comprising, before depositing an insulating material in the at least one second trench and in the semiconductive material recess of the at least one first trench, depositing a second insulating layer over the at least one second trench and over the semiconductive material recess of the at least one first trench.

6. (Original) The method according to Claim 5, wherein depositing the second insulating layer comprises:

forming a thin silicon dioxide layer over the at least one second trench and over the semiconductive material recess of the at least one first trench; and

forming a thin silicon nitride layer over the thin silicon dioxide layer.

7. (Original) The method according to Claim 1, wherein depositing the semiconductive material comprises:

depositing the semiconductor material in the at least one first trench and over the workpiece; and

recessing the semiconductor material below the workpiece top surface.

8. (Original) The method according to Claim 1, wherein the at least one second trench has a greater width than a width of the at least one first trench.

9. (Original) The method according to Claim 1, wherein the semiconductive material recess has a depth below the top surface of the workpiece that is greater than, less than, or equal to the at least one second trench second depth.

10. (Original) A method of forming isolating regions of a semiconductor device, the method comprising:

providing a workpiece, the workpiece having at least one first region and at least one second region, the at least one first region comprising at least one high voltage active area, the second region comprising areas for at least one low voltage active area, the workpiece having a top surface;

patterning the first region with at least one deep trench, the deep trench having sidewalls, a bottom, and a first depth within the workpiece;

forming a first insulating layer over the at least one deep trench sidewalls and bottom;

depositing a semiconductive material in the at least one deep trench over the first insulating layer, wherein the semiconductive material is recessed beneath the workpiece top surface;

masking the at least one first region;

patterning the at least one second region with at least one shallow trench, the shallow trench having a second depth within the workpiece, wherein the second depth is less than the first depth;

removing the mask over the at least one first region;

depositing an insulating material in the at least one shallow trench and in the semiconductive material recess of the at least one deep trench; and

forming at least one low voltage active region in the second region.

11. (Original) The method according to Claim 10, wherein depositing an insulating material in the semiconductive material recess of the at least one deep trench comprises forming shallow trench isolation over the deep trenches.

12. (Original) The method according to Claim 10, wherein depositing the semiconductive material comprises depositing doped polysilicon or undoped polysilicon, wherein forming the insulating layer over the at least one deep trench sidewalls and bottom comprises:

forming a thin nitride layer over the at least one deep trench sidewalls and bottom; and

forming a thin oxide layer over the thin nitride layer.

13. (Original) The method according to Claim 10, further comprising, before depositing an insulating material in the at least one shallow trench and in the semiconductive material recess of

the at least one deep trench, depositing a second insulating layer over the at least one shallow trench and over the semiconductive material recess of the at least one deep trench.

14. (Original) The method according to Claim 13, wherein depositing the second insulating layer comprises:

forming a thin oxide layer over the at least one shallow trench and over the semiconductive material recess of the at least one deep trench; and

forming a thin nitride layer over the thin silicon dioxide layer.

15. (Original) The method according to Claim 10, wherein depositing the semiconductive material comprises:

depositing the semiconductor material in the at least one deep trench and over the workpiece; and

recessing the semiconductor material below the workpiece top surface.

16. (Original) The method according to Claim 10, wherein the at least one shallow trench in the second region has a greater width than a width of the at least one deep trench in the first region.

17. (Original) The method according to Claim 10, wherein a depth of the semiconductive material recess is greater than, less than, or equal to the at least one shallow trench second depth.

18. (Original) The method according to Claim 10, wherein patterning the first region with at least one deep trench comprises:

depositing a hard mask over the workpiece top surface;

patterning the hard mask with the deep trench pattern;

patterning the workpiece using the hard mask as a mask; and

removing the hard mask.

19. (Original) The method according to Claim 18, wherein depositing the hard mask comprises depositing Boron-doped Silicon Glass (BSG).

20. (Original) The method according to Claim 10, wherein masking the at least one first region and patterning the at least one second region with at least one shallow trench comprise:

depositing a hard mask over the workpiece and the patterned deep trench in the first region;

depositing a photoresist over the hard mask;

patterning the photoresist with the at least one shallow trench pattern;

patterning the hard mask with the photoresist pattern;

removing the photoresist;

patterning the workpiece using the hard mask as a mask; and

removing the hard mask.

21. (Currently Amended) The method according to Claim 20, wherein depositing the hard mask comprises depositing high density plasma (HDP) silicon dioxide ~~oxide~~.

22. (Original) A semiconductor device, comprising:

a workpiece, the workpiece having at least one first region including at least one high voltage active area and at least one second region including at least one low voltage active areas, the workpiece having a top surface;

at least one deep trench disposed within the at least one first region proximate a high voltage active area, the deep trench having sidewalls and a bottom, the deep trench including a first insulating layer disposed over the sidewalls and bottom and a semiconductive material disposed over the first insulating layer, the semiconductive material being recessed beneath the workpiece top surface, a shallow isolation region disposed within the semiconductive material recess; and

at least one shallow isolation region disposed within the at least one second region of the workpiece proximate a low voltage active area.

23. (Original) The semiconductor device according to Claim 22, wherein the shallow isolation region of the at least one second region comprises a width greater than the width of the shallow isolation region of the at least one deep trench in the first region.

24. (Original) The semiconductor device according to Claim 22, wherein the semiconductive material recess has a depth greater than, less than, or equal to the depth of the at least one second trench within the workpiece.